REMARKS

The following remarks are made in response to the Final Office Action mailed February 23, 2005. Claims 1-24 and 27 were rejected. With this Response, claim 27 has been cancelled. Claims 1-24 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102

Claim 27 is rejected under 35 U.S.C. 102(e) as being anticipated by Bui, U.S. Patent No. 6,763,478 (Bui). With this Response, Applicant has cancelled claim 27.

Claim Rejections under 35 U.S.C. § 103

Claims 1-24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui in view of Pecone U.S. Patent No. 5,581,693 (Pecone).

Applicant submits that it would not be obvious to one skilled in the art to combine the teachings of Bui either alone or in view of the secondary reference Pecone and arrive at the present invention of claims 1-24.

Independent claim 1 recites a portable computer having a first power mode and a second power mode. The portable computer includes a first memory bus and a second memory bus. A control system is coupled to the first memory bus and the second memory bus, wherein the control system is configured to operate the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different than the first speed in the second power mode.

Bui discloses a computer system that includes a high performance clock frequency and a low performance clock frequency depending on whether battery or AC power is used (See abstract). The computer system includes a NORTH BRIDGE ASIC 30 in communication with SD RAM memory 90 via memory bus 95. (See Bui, Figure 2). When operating in low performance, FSB105 bus frequency and memory bus 95 frequency will be set to 66 MHz. In high performance mode the two buses will operate at 100 MHz. See Bui, column 5, lines 10-13.

Pecone discloses a method and apparatus for inhibiting a computer interface clocks during diagnostic testing. Pecone merely recites a computer system S having a random access memory 114 (RAM) and a read only memory 116 (ROM). See column 3, lines 64, 65. Memory 114 and Memory 116 are shown connected to a common bus 112. See Pecone, Figure 1.

Bui fails to disclose **a second memory bus**. See Examiner's Remarks Final Office Action, Page 4. Further, Bui fails to disclose a **control system coupled to the first memory bus and the second memory bus, wherein the control system is configured to operate the first memory bus and the second memory bus at a first speed in the first power mode and a second speed different than the first speed in the second power mode.**

Pecone fails to disclose a first memory bus and a second memory bus. In contrast, Pecone shows RAM 114 and ROM 116 with a common bus. **Pecone** also fails to disclose a **control system coupled to the first memory bus and the second memory bus, wherein the control system is configured to operate the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different than first speed in the second power mode.** The Examiner states it is will known in the art to have more than one memory in a system, and further states that Pecone clearly discloses that it is common in a computer system to have more than one memory bus. See Final Office Action, page 4. Again, Pecone merely shows RAM 114 and ROM 116 coupled to a common bus 112.

Neither Bui nor Pecone disclose, teach or suggest **a control system configured to operate the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different than the first speed in the second power mode.** Again, Bui discloses ASIC 30 coupled to SD RAM Memory 90 via memory bus 95. Pecone discloses what appears to be ROM 116 and RAM 114 in communication with a common bus 112. Accordingly, one could not combine the teachings of Bui either alone or in combination with the teachings of Pecone and arrive at the present invention of independent claim 1. Similar limitations are included in independent claims 11, 17 and 21. Accordingly, Applicant requests that the above rejection of independent claims 1, 11, 17 and 21 under 35 U.S.C. § 103 be withdrawn.

Dependent claims 2-10, 12-16, 18-20 and 22-24 depend either directly or indirectly upon corresponding independent claims 1, 11, 17 and 21. Dependent claims 2-10, 12-16, 18-20 and 22-24 further define over the art of record. Accordingly, Applicant believes these dependent claims are also allowable.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-24 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-24 is respectfully requested.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either Gregg W. Wisdom at Telephone No. (360) 212-8052, Facsimile No. (360) 212-3060 or Steven E. Dicke at Telephone No. (612) 573-2002, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 25 day of April, 2005.

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